

**SUMMARY DOCUMENT WITH STATUS OF CLAIMS**

**IN THE CLAIMS:**

1 Claim 1 (currently amended): A memory structure comprising:

2 a plurality of adjacent substrates stacked one on another;

3 a plurality of connectors connecting said substrates to one another; [and]

4 [at least one] a memory chip package mounted on each of said substrates[.]; and

5 a gap between a top of said memory chip package and a bottom of an adjacent substrate,

6 wherein said connectors have a size sufficient to form a [gap] space between said

7 substrates, and

8 wherein said [gap] space is larger than a height of said memory chip package.

1 Claim 2 (original): The memory structure in claim 1, wherein said memory chip package

2 comprises a pre-tested memory chip package that is tested for defects before being mounted on

3 said substrates.

1 Claim 3 (original): The memory structure in claim 1, wherein said memory chip package and

2 said substrates include identical electrical connections.

1 Claim 4 (original): The memory structure in claim 1, wherein each of said substrates has a

2 plurality of said memory chip packages mounted thereon.

1 Claim 5 (original): The memory structure in claim 1, wherein said connectors comprises solder

2 balls.

1 Claim 6 (currently amended): The memory structure in claim 1, further comprising a thermal  
2 [connection] material between a top of said memory chip package and a bottom of an adjacent  
3 substrate[, such that said thermal connection fills said gap].

1 Claim 7 (original): The memory structure in claim 1, wherein said memory chip package  
2 comprises a chip having an array of memory elements mounted within a package.

1 Claim 8 (currently amended): A memory structure comprising:  
2 a plurality of adjacent substrates stacked one on another;  
3 a plurality of connectors connecting said substrates to one another; [and]  
4 [at least one] a memory chip package mounted on each of said substrates[,]; and  
5 a gap between a top of said memory chip package and a bottom of an adjacent substrate,  
6 wherein said connectors have a size sufficient to form a [gap] space between said  
7 substrates,  
8 wherein said [gap] space is larger than a height of said memory chip package, and  
9 wherein each memory chip package includes only a single memory chip.

1 Claim 9 (original): The memory structure in claim 8, wherein said memory chip package  
2 comprises a pre-tested memory chip package that is tested for defects before being mounted on  
3 said substrates.

1 Claim 10 (original): The memory structure in claim 8, wherein said memory chip package and  
2 said substrates include identical electrical connections.

1 Claim 11 (original): The memory structure in claim 8, wherein each of said substrates has a  
2 plurality of said memory chip packages mounted thereon.

1 Claim 12 (original): The memory structure in claim 8, wherein said connectors comprise solder  
2 balls.

1 Claim 13 (currently amended): The memory structure in claim 8, further comprising a thermal  
2 [connection] material between a top of said memory chip package and a bottom of an adjacent  
3 substrate[, such that said thermal connection fills said gap and said memory chip package  
4 includes a single memory chip].

1 Claim 14 (original): The memory structure in claim 8, wherein said memory chip package  
2 comprises a chip having an array of memory elements mounted within a package.

Claims 15-20 (cancelled without prejudice or disclaimer)

1 Claim 21 (new): A vertically stacked memory module comprising:  
2 a plurality of adjacent substrates stacked one on another;

3 a plurality of substrate spacers electrically connecting said substrates with one another;  
4 a single memory chip package mounted on each of said substrates;  
5 a plurality of package spacers connecting said memory chip package with said substrates;  
6 and  
7 a gap between a top of said memory chip package and a bottom of an adjacent substrate,  
8 wherein said memory chip package comprises a memory chip having an array of memory  
9 elements mounted within said package,  
10 wherein said substrate spacers form a space between a top of said memory chip package  
11 and a bottom of said adjacent substrates, and  
12 wherein said space is greater than a height of said memory chip package.

1 Claim 22 (new): The memory module in claim 21, wherein said memory chip package  
2 comprises a pre-tested memory chip package that is tested for defects before being mounted on  
3 said substrates.

1 Claim 23 (new): The memory module in claim 21, wherein said memory chip package and said  
2 substrates include identical electrical connections.

1 Claim 24 (new): The memory module in claim 21, wherein each of said substrates has a plurality  
2 of said memory chip packages mounted thereon.

1 Claim 25 (new): The memory module in claim 21, wherein said substrate spacers and said

2 package spacers comprise solder balls.

1 Claim 26 (new): The memory module in claim 21, further comprising thermal material between  
2 a top of said memory chip package and a bottom of an adjacent substrate.